

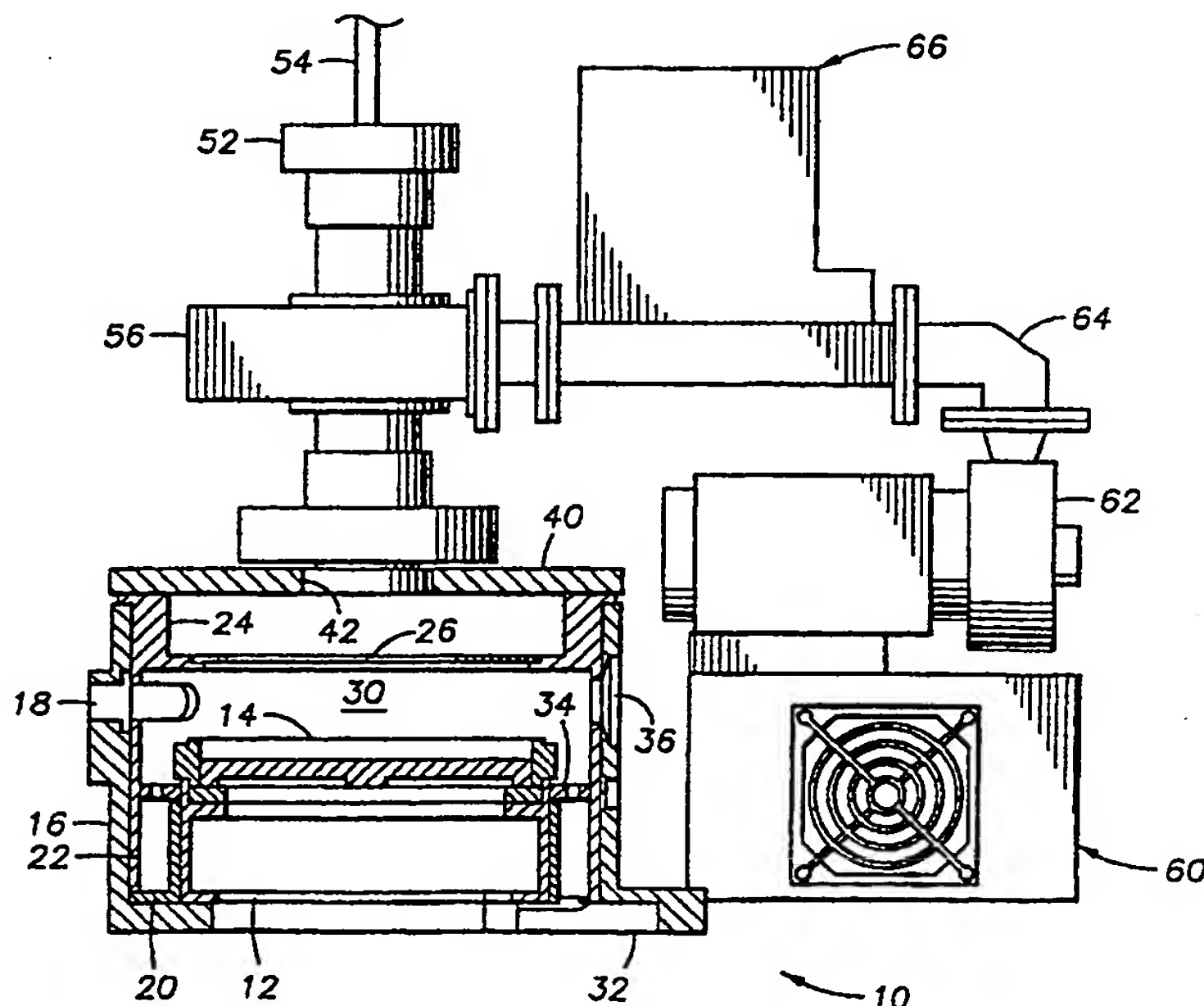
PCTWORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H01L 21/311, 21/3213, C23C 16/02, H01L 21/768		A1	(11) International Publication Number: WO 99/34424 (43) International Publication Date: 8 July 1999 (08.07.99)
(21) International Application Number: PCT/US98/23353 (22) International Filing Date: 2 November 1998 (02.11.98) (30) Priority Data: 09/000,746 30 December 1997 (30.12.97) US (71) Applicant: APPLIED MATERIALS, INC. [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US). (72) Inventors: SUBRAHMANYAN, Suchitra; 988 Alpine Terrace #4, Sunnyvale, CA 94086 (US). CHEN, Liang-Yuh; 1400 Melbourne Street, Foster City, CA 94404 (US). MOSELY, Roderick, Craig; 4337 Diavila Avenue, Pleasanton, CA 94588 (US). (74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).			(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>

(54) Title: PRECLEANING STEP PRIOR TO METALLIZATION FOR SUB-QUARTER MICRON APPLICATION**(57) Abstract**

The present invention generally provides a precleaning process prior to metallization for submicron features on substrates. The method includes cleaning the submicron features with radicals from a plasma of a reactive gas such as oxygen, a mixture of CF_4/O_2 , or a mixture of He/NF_3 , wherein the plasma is preferably generated by a remote plasma source and the radicals are delivered to a chamber in which the substrate is disposed. Native oxides remaining in the submicron features are preferably reduced in a second step by treatment with radicals from a plasma containing hydrogen. Following the first or both precleaning steps, the features can be filled with metal by available metallization techniques which typically include depositing a barrier/liner layer on exposed dielectric surfaces prior to deposition of aluminum, copper, or tungsten. The precleaning and metallization steps can be conducted on available integrated processing platforms.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Larvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

PRECLEANING STEP PRIOR TO METALLIZATION FOR SUB-QUARTER MICRON APPLICATION

BACKGROUND OF THE INVENTION**Field of the Invention**

The present invention relates to a metallization method for manufacturing semiconductor devices. More particularly, the present invention relates to precleaning of submicron features prior to metallization.

Background of the Related Art

Sub-half micron multilevel metallization is one of the key technologies for the next generation of very large scale integration (VLSI). The multilevel interconnects that lie at the heart of this technology require planarization of interconnect features formed in high aspect ratio apertures, including contacts, vias, lines or other features. Reliable formation of these interconnect features is very important to the success of VLSI and to the continued effort to increase circuit density and quality on individual substrates and die.

The increase in circuit densities primarily results from a decrease in the widths of vias, contacts and other features as well as a decrease in the thickness of dielectric materials between these features. Cleaning of the features to remove contaminants prior to metallization is required to improve device integrity. The decrease in width of the features results in larger aspect ratios for the features and increased difficulty in cleaning the features prior to filling the features with metal or other materials. Failure to clean the features can result in void formation within the features or an increase in the resistance of the features. Therefore, there is a great amount of ongoing effort being directed at cleaning small features having high aspect ratios, especially where the ratio of feature height to width is 4:1 or larger.

The presence of native oxides and other contaminants within a small feature typically results in voids by promoting uneven distribution of the depositing metal. The native oxide typically forms as a result of exposing the exposed film layer/substrate to oxygen. Oxygen exposure occurs when moving substrates between processing chambers at atmospheric conditions, or when the small amount of oxygen remaining in

a vacuum chamber contacts the wafer/film layer, or when a layer is damaged by etching. Other contaminants within the features can be sputtered material from an oxide over-etch, residual photoresist from a stripping process, leftover polymer from a previous oxide etch step, or redeposited material from a preclean sputter etch process. The native oxide and other contaminants create regions on the substrate which interfere with film formation, by creating regions where film growth is stunted. Regions of increased growth merge and seal the small features before regions of limited growth can be filled with the depositing metal.

The presence of native oxides and other contaminants also can increase the via/contact resistance and can reduce the electromigration resistance of small features. The contaminants can diffuse into the dielectric layer, the sublayer, or the deposited metal and alter the performance of devices which include the small features. Although contamination may be limited to a thin boundary region within the features, the thin boundary region is a substantial part of the small features. The acceptable level of contaminants in the features decreases as the features get smaller in width.

Precleaning of features using sputter etch processes is effective for reducing contaminants in large features or in small features having aspect ratios smaller than about 4:1. However, sputter etch processes can damage silicon layers by physical bombardment, sputter deposit Si/SiO₂ onto sidewalls of the features, and sputter metal sublayers, such as aluminum or copper, onto sidewalls of the features. For larger features, the sputter etch processes typically reduce the amount of contaminants within the features to acceptable levels. For small features having larger aspect ratios, sputter etch processes have not been as effective in removing contaminants within the features, thereby compromising the performance of the devices which are formed.

Preclean by sputter etch process is particularly unsuitable for features with copper substrate. It is because of the ease of diffusion of sputtered Cu through the dielectric sidewalls. This diffusion is especially true for TEOS, thermal oxide and some low K dielectric materials. Therefore, a new preclean process without any bias on the substrate is needed for a Cu preclean application.

Wet chemical cleaning processes have been developed to clean submicron features prior to metallization without the damage or contamination seen in sputter etch processes. The wet chemical processes typically include treatment of the feature with

hydrofluoric acid (HF) to remove native oxides. Various other wet chemical processes can be used depending on the contaminants remaining in the features. The wet chemical cleaning processes can be combined with dry cleaning processes. However, the addition of wet chemical cleaning steps to remove trace amounts of contaminants from the features substantially increases the overall process time for metallization.

A soft etch cleaning process for submicron features is described by Sumi et al., "New Contact Process Using Soft Etch for Stable Ohmic Characteristics and its Application to 0.1 micron CMOS Devices", IEDM 94-113 et seq. The soft etch process uses an inductively coupled plasma of argon to remove native oxides from a silicon underlayer. The process does not avoid resputtering of materials from the bottom to the sidewalls of the contact hole.

A dry cleaning process for submicron features is described by Taguwa et al., "Low-Contact Resistance Metallization for Gigabit Scale DRAMs Using Fully-Dry Cleaning by Ar/H₂ ECR Plasma", IEDM 95-695 et seq. The dry cleaning process preferably cleans the features with an Electron Cyclotron Plasma containing a mixture of argon and hydrogen prior to chemical vapor deposition of titanium. The cleaning process reduces bombardment by Ar, removes native oxides from a silicon underlayer, and promotes formation of a uniform TiSi_x layer between the silicon underlayer and the deposited titanium. However, addition of H₂ to Ar in the cleaning process does not completely eliminate resputtering of materials within the features.

For sub-quarter micron features having high aspect ratios, resputtering of material from the bottom to the sidewalls of the feature during dry cleaning results in a significant narrowing of the feature and a corresponding increase in resistance of the feature which impairs device performance. The known dry cleaning processes are not effective in removing contaminants from the features without redepositing material on the sidewalls of the features. Therefore, there remains a need for a cleaning process for small features which effectively cleans the feature without leaving contaminants in the feature.

SUMMARY OF THE INVENTION

The present invention provides a method for precleaning features on a semiconductor substrate to remove contaminants prior to metallization. The method

includes removal of oxides from the bottom of contacts without damaging the underlying layer, including the removal of SiO_2 , aluminum oxide or copper oxide from the bottom of vias without redeposition of the material onto sidewalls, the removal of a thin layer of damaged silicon from the bottom of contact holes, and the removal of contaminants from the sidewalls of the features. The precleaning of the features preferably includes a first step wherein contaminants are removed with radicals from a remote plasma of a reactive cleaning gas, and an optional second step wherein native oxides remaining in the features are reduced by exposure to hydrogen radicals. The plasma of the cleaning gas is preferably generated by a remote plasma source to provide a soft etch which does not damage or resputter the sublayers at the bottom of the features.

Following the first or both precleaning steps, the features can be filled with metal by available techniques which typically include depositing a barrier/liner layer on the exposed dielectric surfaces using physical vapor deposition, chemical vapor deposition, or other techniques, prior to deposition of a metal such as aluminum (Al), copper (Cu), or tungsten (W) to completely fill the feature. The precleaning and metallization steps can be conducted on available integrated processing platforms such as the Endura[®] system available from Applied Materials, Inc., Santa Clara, California.

In one aspect of the invention, submicron features formed in a dielectric layer on a semiconductor substrate are processed by precleaning the submicron features with radicals from a plasma comprising a reactive gas such as oxygen, a mixture of CF_4/O_2 , or a mixture of He/NF_3 , wherein the plasma is generated by a remote plasma source and neutral radicals are delivered into a chamber containing the substrate. Subsequent to cleaning with the reactive gas, native oxides remaining in the submicron features are removed with radicals from a plasma comprising hydrogen alone or in mixtures with nitrogen (N), argon (Ar), or helium (He). The hydrogen radicals also remove carbon and fluorine contaminants in addition to oxides. Following precleaning, a liner or barrier layer is preferably deposited on exposed surfaces of the feature, and the feature is then filled with Al, Cu, W, or other conductive material. When the liner or barrier layer is Ti or Ti/TiN, deposition of the titanium at 650-750°C on a silicon surface precleaned according to the present invention forms a uniform, one phase layer of TiSi_x . Precleaning can also be performed *in situ* in a CVD TiN chamber which deposits a

barrier layer for copper or aluminum metallization by addition of a remote plasma source to the chamber.

In another aspect of the invention, precleaning according to the present invention can be performed both before and after deposition of a barrier layer to reduce the amount of contaminants on both sides of the barrier layer and improve the electromigration resistance of the feature.

BRIEF DESCRIPTION OF THE DRAWINGS

So that the manner in which the above recited features, advantages and objects of the present invention are attained can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

Figure 1 shows a reactive preclean chamber which receives a remote plasma source to conduct the precleaning steps of the present invention;

Figure 2 shows the overall layout of an inductively coupled plasma reactor which generates a plasma to conduct the precleaning steps of the present invention;

Figure 3 is a schematic top view in section along lines 3-3 of Fig. 2 showing the gas distribution system;

Figure 4 is a schematic enlarged view showing the gas distribution system of Figure 2;

Figure 5 shows an integrated processing platform configured to preclean and fill features on a semiconductor substrate according to the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The present invention generally provides a method of precleaning features etched into a dielectric layer on a semiconductor substrate, the method comprising the steps of precleaning the submicron features with radicals from a plasma comprising a reactive gas, wherein the plasma is preferably generated by a remote plasma source and neutral radicals are delivered into a chamber having the substrate disposed therein.

Native oxides remaining in the submicron features after remote plasma treatment are preferably reduced by reaction with hydrogen prior to metallization of the feature. More particularly, the present invention provides precleaning of the submicron features and filling of the features with a metal such as copper, aluminum, or tungsten. The process steps can be combined in an integrated processing system, such as the Endura® system available from Applied Materials, Inc., Santa Clara, California, although non-integrated techniques can be used to clean and fill submicron features in accordance with the present invention.

For clarity, the present invention will be described below with reference to both copper and aluminum deposition techniques. However, tungsten or other metal deposition processes may be used to accomplish the advantages of the present invention, whether presently known or yet to be discovered.

The invention provides a suitable method for precleaning vias, contacts, and other features etched into a dielectric layer, such as a silicon dioxide layer, which is deposited on a conductive or semi-conductive sublayer, such as Ge, Si, Al, Cu, or TiN sublayers. The feature typically exposes the sublayer so that the feature can be filled with a conductive or semi-conductive material which connects the sublayer and a subsequent metal interconnect layer to be deposited on the dielectric layer. Etching of the features in the dielectric typically leaves contaminants which should be removed to improve filling of the features and ultimately improve the integrity and reliability of the devices formed.

After etching of the dielectric layer, the features can have damaged silicon or metal residues within the features from over-etching of the dielectric layer. The features can also contain residual photoresist on the feature surfaces from the photoresist stripping and/or ashing process or residual polymer from the dielectric etch step. The features may also contain redeposited material on the feature surfaces following a sputter etch preclean process. These contaminants can migrate into the dielectric layer or can interfere with the selectivity of metallization by promoting uneven distribution of the depositing metal. The presence of the contaminants also can increase the resistance of the deposited metal by substantially narrowing the width of the feature, and thus creating a narrowed portion in the metal forming the via, contact line, or other conductive feature.

The submicron features which are cleaned and filled in accordance with the present invention, are formed by conventional techniques which deposit a dielectric material over a surface on a semiconductor substrate. Any dielectric material, whether presently known or yet to be discovered, may be used and is within the scope of the present invention, including low dielectric materials such as organic polymers and aerogels. The dielectric layer may comprise one or more distinct layers and may be deposited on any suitable deposition enhancing sublayer. The preferred deposition enhancing sublayers include conductive metals such as Al and Cu, barrier surfaces such as TiN, and doped silicon.

Once deposited, the dielectric layer is etched by conventional techniques to form vias, contacts, trenches or other submicron features. The features will typically have a high aspect ratio with steep sidewalls. Etching of the dielectric layer may be accomplished with any dielectric etching process, including plasma etching. Specific techniques for etching silicon dioxide include such compounds as buffered hydrofluoric acid and acetone. However, patterning may be accomplished on any layer using any method known in the art.

A Preferred Precleaning Apparatus

The precleaning process of the present invention is preferably conducted on a remote plasma source (RPS) chamber such as the Etch RPS chamber which is available from Applied Materials, Inc., Santa Clara, California. The chamber comprises two major assemblies: 1) a chamber body, preferably, but not necessarily, including an electrostatic chuck which supports and secures a substrate in the chamber; and 2) a remote plasma source. These major assemblies will be discussed separately for the sake of organization, although it will be understood that in reality there is dynamic interaction between these assemblies. In a RPS chamber, reactive H radicals are formed by the remote source and are introduced into the neighborhood of the substrate as primarily neutral species, *i.e.*, not having an electric charge and therefore not an ion, thereby preventing generation of self bias and bombardment of the wafer surface by ions. Experiments with RPS chambers show that a 2.45 GHz microwave source is more efficient and can generate more hydrogen radicals than lower frequency RF sources.

Chamber Body/Electrostatic Chuck Assembly

Referring to Figure 1, features etched on a substrate are precleaned in a remote plasma source (RPS) chamber 10 having a fixed cathode 12 which includes an electrostatic chuck 14 that secures the substrate (not shown) to the fixed cathode 12. The chamber 10 includes a chamber body 16 having a slit valve port 18 which connects the chamber 10 to a substrate processing platform such as the Endura® platform.

The fixed cathode 12 is shielded from process gases by a cathode liner 20 which has a non-stick outer surface to enhance process performance. The chamber body 16 is also shielded from process gases by a chamber liner 22 which has a non-stick inner surface to enhance process performance. The chamber liner 22 includes an inner annular ledge 24 which supports a gas distribution plate 26. The gas distribution plate 26 has a plurality of spaced holes which distribute process gases received from a remote plasma source described below. The process gases flow over the surface of a substrate positioned on the electrostatic chuck 14. The remote plasma source typically confines any plasma of the process gases and provides neutral radicals to the chamber 22. The gas distribution plate may be grounded to further reduce ions remaining in the process gases.

A processing region 30 above the fixed cathode 12 is maintained at a low process pressure by vacuum pumps (not shown) which are in fluid communication with an exhaust port 32 on the chamber body 16. A plenum 34 having a plurality of spaced holes separates the processing region 30 from the exhaust port 32 to promote uniform exhausting around the fixed cathode 12. The processing region 30 is visible from outside the chamber 10 through a sapphire window 36 which is sealed in the chamber body 16.

The chamber 10 has a removable chamber lid 40 which rests on the chamber liner 22. The chamber lid 40 has a central injection port 42 which receives process gases from a remote plasma source 50 described below.

Remote Plasma Source

Referring to Figure 1, process gases for the precleaning process of the present invention are excited into a plasma within a remote plasma source 50 which is in fluid

communication with the RPS chamber 10 described above. A plasma applicator 52 has a gas inlet 54 which receives process gases. The process gases flow through the applicator 52 and exit into the central injection port 42 in the chamber lid 40. A jacket waveguide 56 surrounds a sapphire tube portion of the plasma applicator 52 and supplies microwave energy to the process gases. The plasma is generated in the applicator 52 and is typically confined to the applicator 52.

Microwave energy is generated by a magnetron 60 which provides up to 1500 watts at 2.45 GHz. The microwave energy passes through a microwave isolator 62 which prevents reflected power from damaging the magnetron 60. The microwave energy from the isolator 62 is transmitted through a 90° waveguide 64 to an autotuner 66 which automatically adjusts the impedance of the plasma in the applicator 52 to the impedance of the magnetron 60 resulting in minimum reflected power and maximum transfer of power to the plasma applicator 52.

The process gases receive sufficient energy in the applicator 52 to form a plasma containing reactive (radical) species. A plasma of CF_4 and O_2 generates O radicals and some F radicals. The process gases are mostly neutralized before leaving the applicator 52. The process gases retain a substantial portion of the radicals after passing through the distribution plate 26. The radicals are delivered over the substrate before the process gases are exhausted from the chamber. The F radical primarily combines with Si and SiO_2 to form volatile SiF_4 . The O radicals combine with fluorocarbons to form CO, CO_2 , and COF_2 . Hydrogen radicals react with the native oxide to form water vapor and the metal. The exhaust carries the various byproducts as well as some of the recombination species.

Although precleaning is shown for a dedicated precleaning chamber in Figure 1, precleaning could also be done by connecting the remote plasma source to a metal CVD/PVD chamber. For example, gas inlets could be provided at the level of the substrate in such metallization chambers to deliver the reactive gas plasma or hydrogen plasma from the remote plasma source. Metal deposition chambers having gas delivery systems could be modified to deliver the precleaning gas plasma through existing gas inlets such as a gas distribution showerhead positioned above the substrate.

The Precleaning Process

The present invention provides a method for precleaning features on a semiconductor substrate to remove contaminants prior to metallization. The method includes removal of silicon dioxide from the bottom of contacts without damaging the silicon, removal of aluminum oxide or copper oxide from the bottom of vias without redeposition of the metal onto sidewalls, removal of a thin layer of silicon from the bottom of contact holes, and removal of contaminants from the sidewalls of the features.

According to the invention, features formed in a dielectric layer on a semiconductor substrate are precleaned with radicals from a plasma comprising a reactive gas such as oxygen, a mixture of CF_4/O_2 , or a mixture of He/NF_3 , wherein the plasma is preferably generated by a remote plasma source and delivered into a chamber in which the substrate is disposed. The preferred reactive gas is CF_4/O_2 which provides both oxygen ions and fluorine ions during the cleaning process. This process typically uses a high concentration of O_2 to form a non-polymerizing mixture for effective removal of fluorine and carbon containing species. The gas mixture can be varied to obtain a wide range of removal etch rates (50 Å/min to 500 Å/min) and a wide range of Si:SiO₂ etch selectivities. The cleaning process leaves native oxides in the features, and the native oxides are preferably reduced in a second step by radicals from a plasma comprising hydrogen, alone or in mixtures with N, Ar or He which function to dilute the reactive radicals. Following the first or both cleaning steps, a liner or barrier layer such as TiN or Ti is preferably deposited on exposed surfaces of the feature, and the feature is preferably filled with a conductive material such as Al, Cu, or W by PVD, CVD, or electroplating processes.

In one aspect of the invention, submicron features formed in a dielectric layer on a semiconductor or metal substrate are processed by precleaning the submicron features with radicals from a plasma comprising a CF_4/O_2 , wherein the plasma is generated by a remote plasma source and delivered into a chamber containing the substrate. The reactive gas radicals remove residual photoresist, hydrocarbons, and fluorocarbons from the sidewalls of the features. The reactive gas radicals can also remove damaged Si on the bottom of the feature. A plasma of CF_4/O_2 contains both fluorine radicals and oxygen radicals. The fluorine radicals remove silicon by the

formation of SiF_4 , which is volatile under process conditions. The fluorine radicals remove silicon dioxide by formation of SiF_4 and CO and other oxygen compounds which are volatile under process conditions. The fluorine radicals also remove hydrogen from hydrocarbon or fluorocarbon contaminants within the feature, and assist the oxygen radicals in breaking down the hydrocarbons and fluorocarbons into volatile components. An inert gas such as helium can be provided in the plasma as desired to dilute the reactive radicals. For features having silicon sublayers, typically the first level, the fluorine radicals preferably remove damaged silicon by removing a small layer, *e.g.*, 50Å, of the silicon.

Subsequent to cleaning with the radicals from the plasma of the reactive gas, native oxides remaining in the submicron features can be reduced with radicals from a plasma comprising hydrogen, alone or in mixtures with N, Ar, or He. Reduction of the native oxides provides an oxygen free interface between the feature and the sublayer which reduces the resistance of the feature. Thermal reduction of the native oxides using hydrogen or hydrogen contains mixture can be achieved in a CVD TiN chamber RPS chamber at 350°C. The hydrogen surface treatment of the native oxides has an added benefit of leaving dangling hydrogen bonds on the surface of the sublayer at the bottom of the feature. The dangling hydrogen bonds help reduce subsequent films which are deposited from carbon based precursors. The hydrogen treatment in the case of a Si sublayer passivates the Si surface, and thereby makes it resistant to reoxidation when exposed to the atmosphere.

Following precleaning according to the invention, a liner or barrier layer is preferably deposited on exposed surfaces of the feature, and the feature is filled with Al, Cu, W, or other conductive material. When the liner or barrier layer is Ti or Ti/TiN, titanium deposited on a silicon surface precleaned according to the present invention forms a uniform, one phase layer of TiSi_x . When the liner or barrier layer is Ti or Ti/TiN, deposition of the titanium at 650-750°C on a silicon surface precleaned according to the present invention forms the uniform, one phase layer of TiSi_x .

In another aspect of the invention, precleaning according to the present invention can be performed both before and after deposition of a barrier layer to increase the electromigration resistance of the deposited Al, Cu, W, or other conductive metal which fills the feature. Preferred barrier/lining layers include such layers as

tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and titanium nitride (TiN), or a combination of these layers. Treatment of barrier/lining layers with H₂ radicals generated by remote plasma or thermal processes can be used to provide better adhesion to CVD deposited Al or CVD deposited Cu. For example, treatment of Ta, TaN, or CVD deposited TiN with H₂ or H₂ gas mixture with He, Ar, or N₂ provides excellent adhesion to copper. The H₂ gas mixtures preferably comprise at least 90% by volume of H₂. This H₂ treatment of the barrier layer can also be done *in situ* in the metal deposition chamber (e.g., Cu) by mounting a remote plasma source to a CVD Cu chamber. This *in situ* treatment passivates the barrier surface and prevents adsorption of C, O, and F compounds leading to better adhesion and lower resistivity of CVD Cu on Ta, TaN, or TiN surfaces. This treatment will also improve the texture, grain orientation, and grain size of Cu on the barrier layer resulting in good surface topography and tighter distribution of grain orientations.

The precleaning method of the invention is especially useful for cleaning of submicron features having copper sublayers at the bottom of the features since copper is easily sputtered to the side walls in a conventional ICP or sputter etch based preclean chamber. The sputtered copper diffuses into the dielectric material causing device failure. The present invention cleans the via without sputtering of the base of the via.

Hypothetical Example

The following hypothetical example describes the preferred method of the present invention by describing the precleaning of features etched into a silicon dioxide layer having a copper sublayer. Precleaning includes a first step of exposing the features to radicals from a plasma of CF₄/O₂ which is generated in a remote plasma source. The radicals are delivered to a chamber in which a substrate having the features is disposed. A plasma comprising hydrogen is then generated to deliver H radicals to the chamber to reduce native oxides, oxides from plasma damage in a previous oxide etch step, or oxides from wet chemistry used after the etch step, prior to filling of the features with copper in a CVD plasma reactor.

The precleaning chamber is stabilized for 5 seconds at a pressure of 400 mTorr with an oxygen flow of 200 sccm and a tetrafluoromethane (CF₄) flow of 10 sccm prior to application of microwave power in the remote plasma source. The features are then

cleaned for 30 seconds by applying 1000 W of microwave power (2.45 GHz) to the remote plasma. Then native oxides are reduced in the features by treatment for 30 seconds with radicals from a hydrogen plasma at a pressure of 350 to 450 mTorr with a hydrogen flow of 300 to 500 sccm and 600 to 1000 W of microwave power (2.45 GHz) to the remote plasma source.

An Alternative Embodiment

Referring now to Figure 2, an alternative processing chamber for conducting the process of the invention is shown schematically in a section view. The processing chamber can be a Preclean II chamber which is available from Applied Materials, Santa Clara, California. A vacuum chamber 111 is formed by a base member 112 having sidewalls 114 and which are preferably made of metallic construction such as stainless steel, aluminum or the like. An opening 115 in the base of the body member 112 is connected to a turbo pump 116 which is used to control the gas pressure inside the chamber 111. A quartz dome 117 forms the top of the chamber 111 and is provided with a flange 18 about its circumference where it mates with the top circumference of the sidewalls 114 of base member 112. A gas distribution system 119 is provided at the juncture of quartz dome 117 and base member 112 which will be discussed in more detail below. An insulating pedestal 120 made of quartz, ceramic or the like has a quartz cover 121 holding down a conductive pedestal 122 which is arranged to hold a wafer in the chamber 111. A high frequency RF power supply 123 is capacitively coupled to the pedestal 122 and supplies a negative bias voltage thereto. This bias voltage is not used during the precleaning steps of the present invention.

A helical shaped RF induction coil 125 is wound exteriorly to quartz dome 117 and is supported by the cover 127. The coil 125 is formed of hollow copper tubing. An alternating axial electromagnetic field is produced in the chamber 111 interiorly to the windings of the coil 125. Generally, an RF frequency of from about 350 KHz to about 450 KHz is employed and an RF power supply of conventional design (not shown) operating at this frequency is coupled to the coil 125 by a matching network (not shown) to generate a plasma in the chamber 111. The RF electromagnetic field generates a glow discharge plasma within the portion of the chamber 111 above the pedestal 122 which has a plasma sheath or dark space separating the plasma from the

pedestal and the wafer.

Referring now to Figures 3 and 4, the gas distribution system for the reactant gas used in the system is shown in more detail, but still schematically. The top of the metallic sidewall member 114 has a gas supply trench 133 milled therein and twelve evenly spaced (angularly) disposed channels extending from a gas source intersect the channel to form a plurality of gas injection holes 132. When the flange 118 of quartz dome 117 is placed over the sidewalls 114 of the base member 112, a closed toroidal tube is formed in the space provided by the groove 133 and capped or topped by the flange 118 of dome 117. The reactant gas (usually fluorine or the like) is thus supplied at about the midpoint of the chamber 111 and is uniform in its flow across the wafer.

Example

The precleaning steps of the present invention have been combined in the chamber shown in Figures 2-4 to successfully clean features etched in a dielectric layer having a copper sublayer prior to filling of the features with a Cu or Al plug. The chamber was stabilized for 5 seconds at a pressure of 5-20 mTorr with a mixture of 90% H₂ and 10% He, Ar, or N₂. The features were then cleaned for 60 seconds by applying 300 W of 400 KHz RF power to the coil and 10 W of RF power (13.56 MHz) to the pedestal. These process conditions (*i.e.* with very low bias) can chemically reduce CuO without sputtering of the Cu sublayer onto the sidewalls. Similar treatment can also be used for Si or TiSi_x sublayers at higher temperatures.

Integrated Processing System

The precleaning process of this invention is conducted in the dedicated precleaning chamber as described above, or done *in situ* in the barrier layer chamber. The precleaning chamber is preferably integrated with other metallization process chambers on a processing platform to avoid interim contamination of the substrates. A preferred integration scheme is shown in Figure 5 which represents various processing chambers mounted on an ENDURA® platform available from Applied Materials, Inc.

Referring to Figure 5, a schematic diagram shows an integrated processing system 160 having a RPS chamber for precleaning of the substrates and both PVD and CVD chambers thereon in which integrated metallization processes can be

implemented. Typically, the substrates are introduced and withdrawn from the processing system 160 through a cassette loadlock 162. A robot 164 having a blade 167 is located within the processing system 160 to move the substrates through the system 160. A first robot 164 is typically positioned in a buffer chamber 168 to transfer substrates between the cassette loadlock 162, degas wafer orientation chamber 170, RPS preclean chamber 172, HP-PVD Ti/TiN chamber 175 and a cooldown chamber 176. A second robot 178 is located in transfer chamber 180 to transfer substrates to and from the cooldown chambers 176, a PVD IMP Ti/TiN chamber 182, a CVD Al Chamber 184, a CVD TiN chamber 186, and a PVD HTHU Al chamber 188. The transfer chamber 180 in the integrated system is preferably maintained at low pressure or high vacuum in the range of 10^{-8} torr. This specific configuration of the chambers in Figure 5 comprise an integrated processing system capable of both CVD and PVD processes in a single cluster tool. This particular chamber configuration or arrangement is merely illustrative and more configurations of PVD and CVD processes are contemplated by the present invention.

Typically, a substrate processed in the processing system 160 is passed from the cassette loadlock 162 to the buffer chamber 168 where the robot 164 first moves the substrate into a degas chamber 170. The substrate is then be transferred into RPS preclean chamber 172, PVD HP TiN chamber 175, and then into a cooldown chamber 176. From the cooldown chamber 176, the robot 178 typically moves the substrate into and between one or more processing chambers before returning the substrate back to a cooldown chamber 176. It is anticipated that the substrate may be processed or cooled in one or more chambers any number of times in any order to fill the submicron features with aluminum. The substrate is removed from the processing system 160, following processing, through the buffer chamber 168 and then to the loadlock 162. A microprocessor controller 190 controls the sequence and formation of the layers on the substrates.

In accordance with the present invention, the processing system 160 passes a substrate through loadlock 162 into de-gas chamber 170 wherein the substrate is introduced to out gas contaminants. A substrate is then moved into the RPS pre-clean chamber 172 where the submicron features are cleaned to remove any contaminants thereon and to reduce native oxides. The substrate is then processed in the PVD HP

Ti/TiN chamber 175 to deposit a Ti/TiN barrier layer on the cleaned dielectric surfaces, and then passed to a cooldown chamber 176. The second robot 178 then transfers the substrate to one or more CVD and PVD chambers for aluminum deposition.

The integrated platform 160 also enables a uniform and single phase deposition of titanium silicide by following the precleaning of a silicon sublayer with Ti deposition in the PVD IMP Ti/TiN chamber 182. After silicidation, warm Al, cool Al, or selective Al deposition completes the metallization of the submicron features.

Another application of the integrated platform of Figure 5 provides for copper deposition by providing a CVD TiN chamber 175, a PVD γ -Cu chamber 182, a CVD Cu chamber 184, a PVD HTHU Cu chamber 186, and a PVD IMP Ta/TaN chamber 188. The substrate is processed in the CVD TiN chamber 175 or PVD IMP Ta/TaN chamber 188 to deposit a CVD TiN or Ta/TaN barrier layer on the cleaned dielectric surfaces, and then the substrate is passed to a cooldown chamber 176. Precleaning of submicron features prior to copper deposition can be performed in an RPS chamber 172 or in a Preclean II chamber which replaces a cooldown chamber 176. The Preclean II chamber modifies a cooldown chamber by addition of H₂, Ar, He, and N₂ plumbing. The second robot 178 then transfers the substrate to one or more CVD and PVD chambers for copper deposition. Deposited Cu layers may be annealed with H₂ to make the layer more resistant to formation of CuO.

Another application of the integrated platform of provides for tungsten deposition by providing a IMP Ti chamber, two CVD TiN chambers, and two preclean chambers. The substrate is processed in the IMP Ti and CVD TiN chambers to deposit Ti/TiN barrier layers on the cleaned dielectric surfaces, and then the substrate is passed to a cooldown chamber. Precleaning of submicron features prior to tungsten deposition can be performed in an RPS based preclean chamber.

A staged-vacuum wafer processing method suitable for use with the present invention is disclosed in United States Patent No. 5,186,718, entitled "Staged-Vacuum Wafer Processing System and Method," Tepman et al., issued on February 16, 1993, which is hereby incorporated herein by reference. This method readily accommodates the precleaning method of this invention. Any combination of processing chambers can be used with the dedicated precleaning chamber.

While the foregoing is directed to preferred embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof. The scope of the invention is determined by the claims which follow.

WHAT IS CLAIMED IS:

1. A method of precleaning features formed in a dielectric layer on a semiconductor substrate, comprising the steps of:
 - a) generating a plasma of a reactive gas in a remote plasma source; and
 - b) delivering radicals from the plasma of the reactive gas to a process chamber which contains the substrate.
2. The method of claim 1, wherein the reactive gas is oxygen, a mixture of CF_4/O_2 , or a mixture of He/NF_3 .
3. The method of claim 1, wherein the radicals of the plasma of a reactive gas is delivered to a barrier layer deposition chamber prior to deposition of a barrier layer.
4. The method of claim 1, wherein the remote plasma source is a microwave source.
5. The method of claim 1, further comprising the step of reducing native oxides with radicals from a plasma comprising hydrogen.
6. The method of claim 5, wherein the native oxide is reduced by radicals from a plasma consisting of hydrogen, or a mixture of hydrogen and N_2 , Ar, or He.
7. The method of claim 1, wherein the radicals from the plasma are delivered to a copper deposition chamber for passivation of a barrier layer prior to copper deposition.
8. A method of forming features on semiconductor substrates, comprising the steps of:
 - a) depositing a dielectric layer on a semiconductor substrate having a surface comprising a conductive or a semiconductive sublayer;
 - b) etching features in the dielectric layer to expose the sublayer;
 - c) cleaning the features with radicals from a plasma of a reactive gas which

comprises oxygen, a mixture of CF_4/O_2 , or a mixture of He/NF_3 , wherein the plasma is generated by a remote plasma source and the radicals are delivered to a chamber which contains the substrate; and

d) filling the features with a conductive or semiconductive material.

9. The method of claim 8, wherein the dielectric layer comprises silicon dioxide.

10. The method of claim 8, wherein the reactive gas is a mixture of CF_4/O_2 .

11. The method of claim 8, wherein a TiSi_x layer is formed within the feature.

12. The method of claim 8, further comprising the step of reducing native oxides remaining in the features with radicals from a plasma comprising hydrogen with little or no bias power applied to the substrate.

13. The method of claim 8, further comprising the steps of depositing a barrier layer of TiN on the feature and cleaning the barrier layer with radicals from a plasma consisting of hydrogen, or a mixture of hydrogen and N_2 , Ar, or He.

14. A method of precleaning and filling submicron features in a dielectric layer on a semiconductor substrate, comprising the steps of:

a) cleaning the submicron features with radicals from a plasma comprising a reactive gas; and

b) reducing native oxides remaining in the submicron features with radicals from a plasma comprising hydrogen.

15. The method of claim 14, wherein the reactive gas is a mixture of CF_4/O_2 .

16. The method of claim 14, further comprising the step of depositing a barrier/liner layer on exposed surfaces of the dielectric layer, wherein the barrier/liner layer comprises a material selected from the group consisting of titanium, titanium nitride, tantalum, and tantalum nitride.

17. The method of claim 16, further comprising the step of cleaning the barrier/liner layer with radicals from a plasma of a reactive gas which comprises oxygen, a mixture of CF_4/O_2 , or a mixture of He/NF_3 .
18. The method of claim 17, further comprising the step of depositing aluminum, copper, or tungsten on the barrier/liner layer.
19. The method of claim 14, wherein the plasma is generated in a remote plasma source and the radicals are delivered to a barrier layer deposition chamber in which contains the substrate prior to deposition of the barrier layer.
20. The method of claim 14, wherein the plasma is generated in a remote plasma source and the radicals are delivered to a copper deposition chamber for passivation of a barrier layer prior to copper deposition.

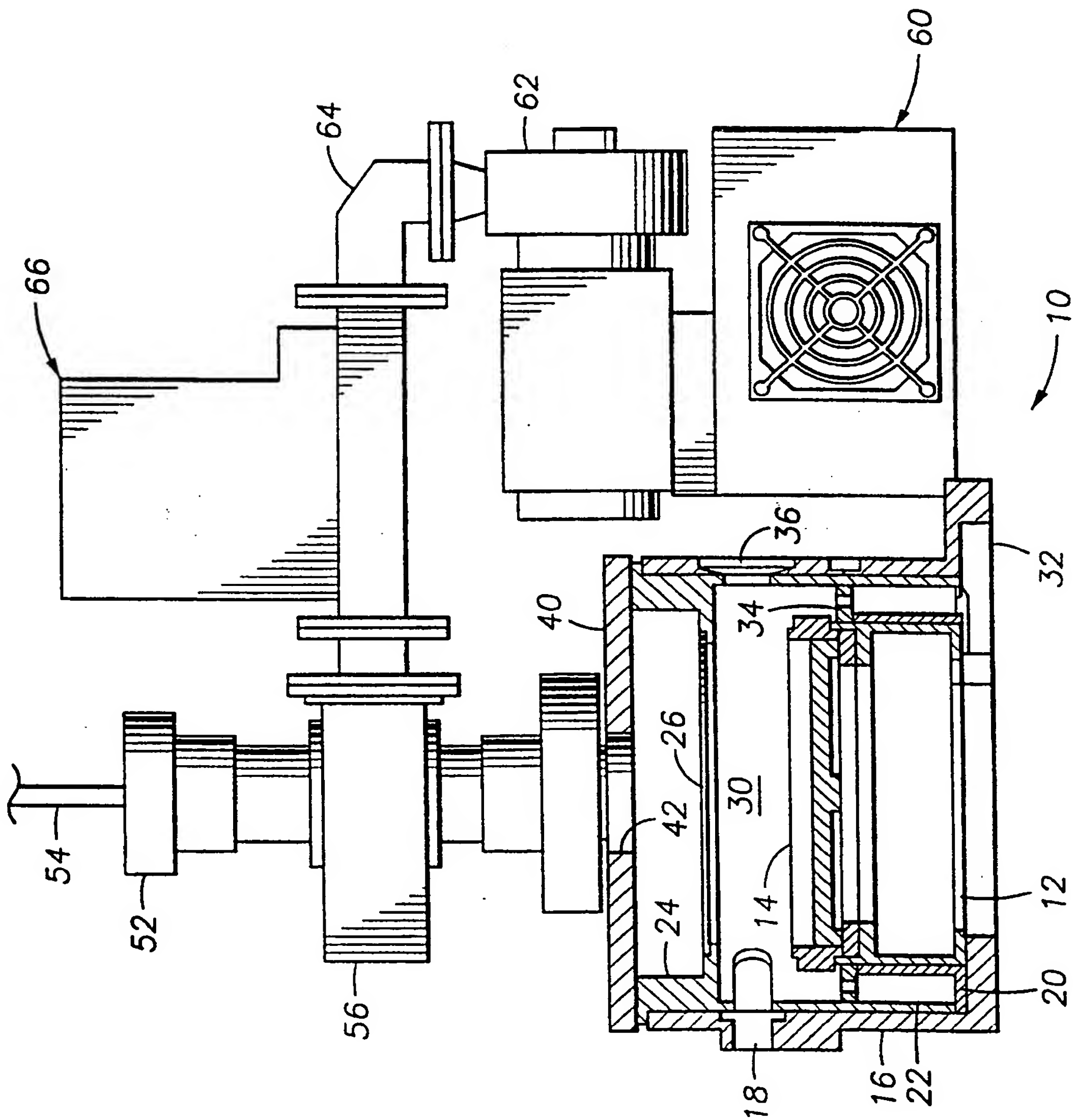


FIG. 1

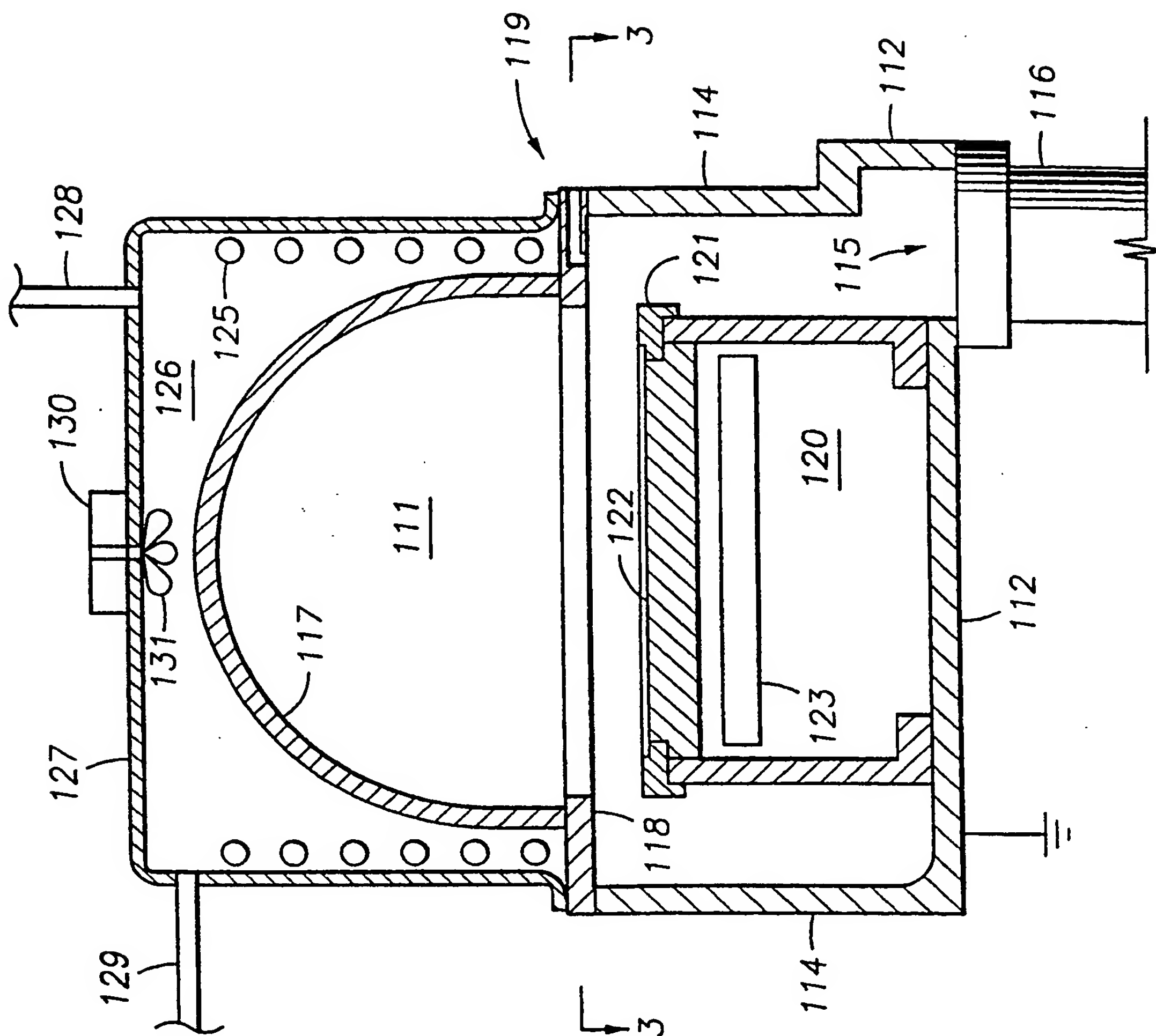
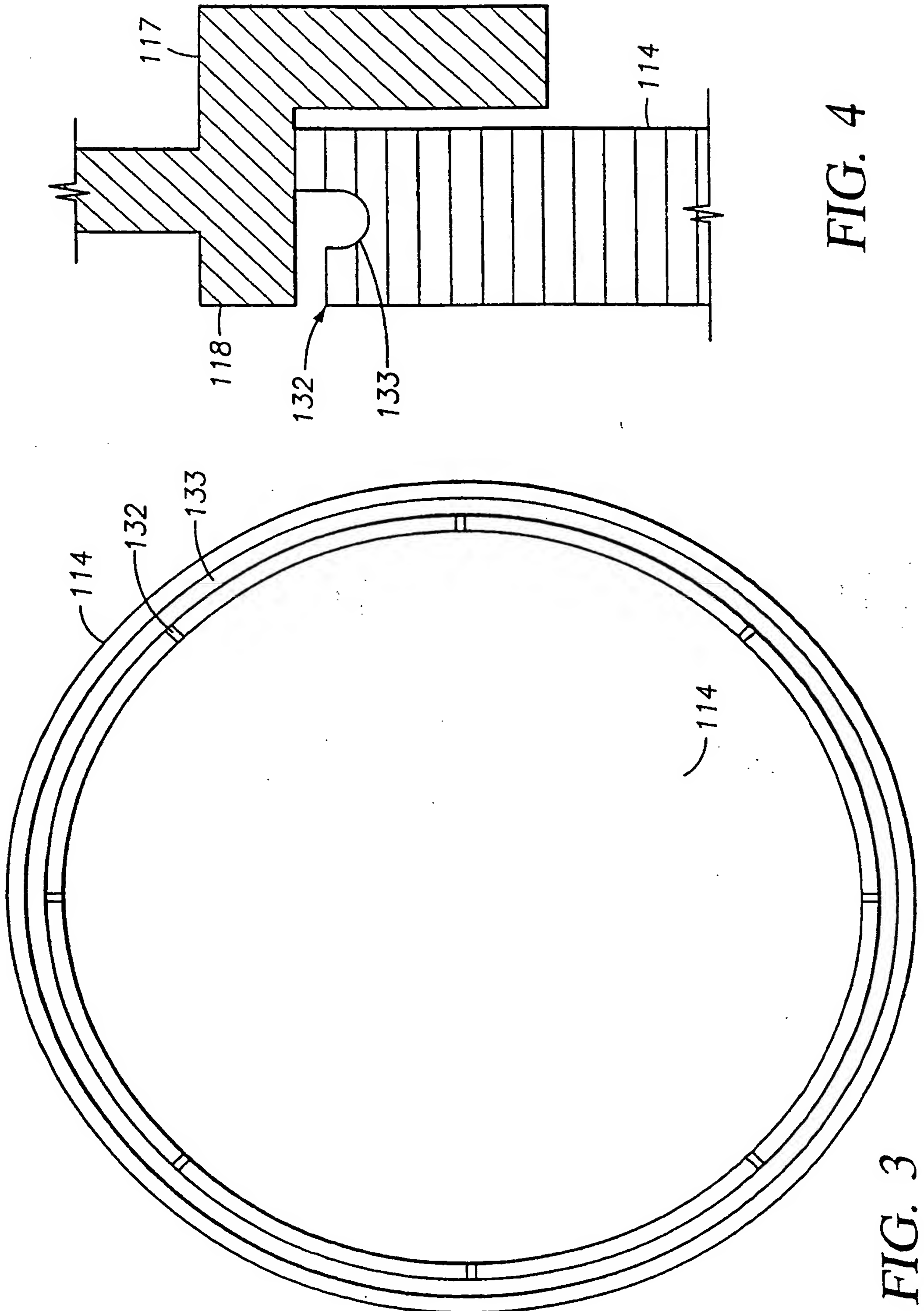


FIG. 2



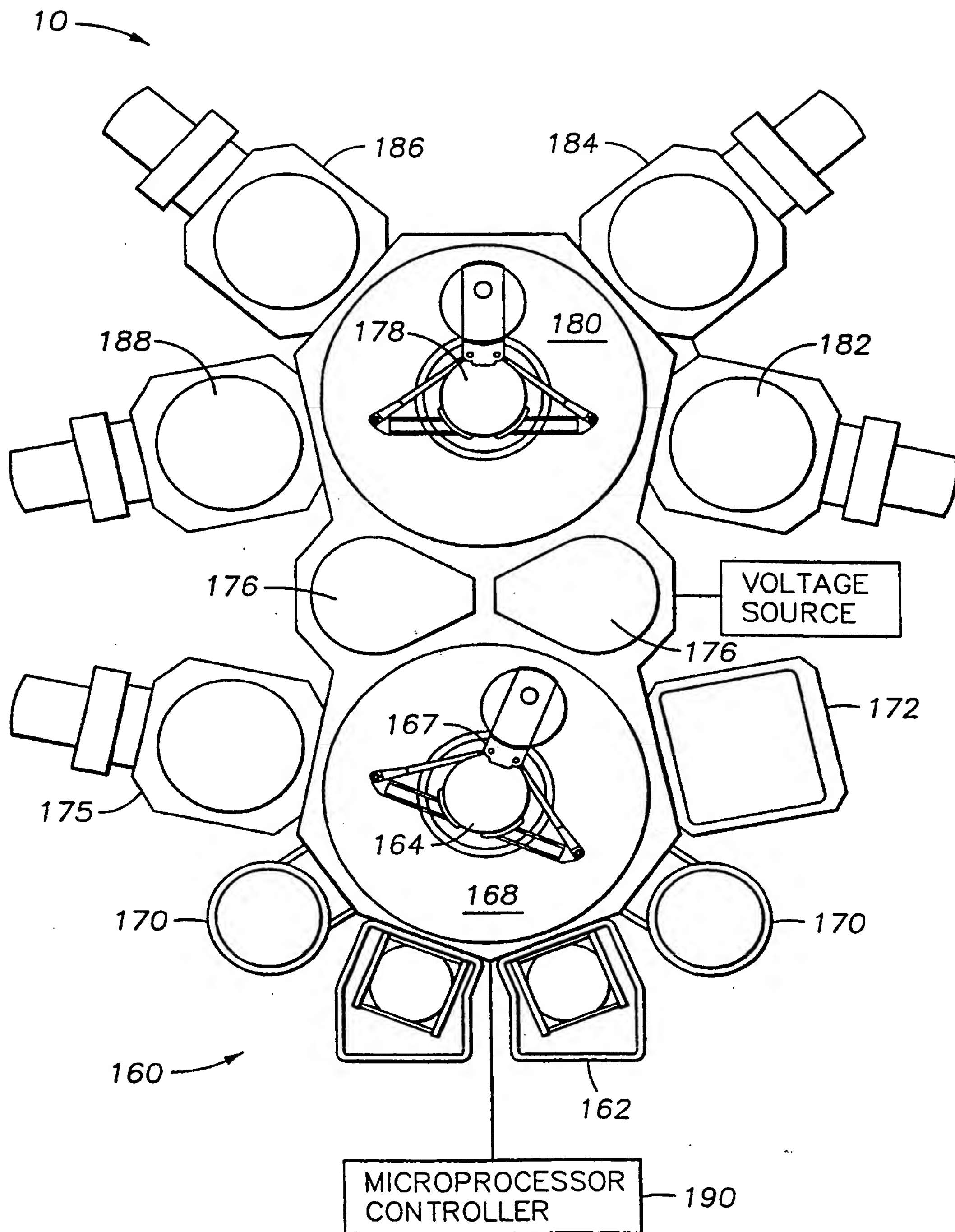


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 98/23353

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H01L21/311 H01L21/3213 C23C16/02 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L C23C G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 305 946 A (TOKYO SHIBAURA ELECTRIC CO) 8 March 1989 see column 1, line 8 - line 26 see column 3, line 30 - line 41 see column 5, line 15 - line 28 see column 8, line 9 - column 10, line 27; figures 3,4 see column 11, line 19 - line 28; figure 6 see column 12, line 51 - column 13, line 46; figure 9 see column 25, line 37 - column 26, line 16; figure 29	1,2,4-6
A	---	3,7-20
	-/--	



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

5 March 1999

Date of mailing of the international search report

15/03/1999

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl.
Fax: (+31-70) 340-3016

Authorized officer

Klopfenstein, P

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 98/23353

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 306 671 A (OGAWA TOSHIKI ET AL) 26 April 1994 see column 1, line 10 - line 16 see column 1, line 44 - column 2, line 62 see column 3, line 1 - line 13 see column 3, line 67 - column 5, line 7; figures 1A-1F, 2 see column 6, line 33 - line 66	1, 2, 4-6
Y		3, 8-12, 14-16, 19
A		7, 13, 17, 18, 20
X	EP 0 518 774 A (FRANCE TELECOM) 16 December 1992 see column 1, line 1 - line 40 see column 2, line 26 - column 3, line 9 see column 3, line 27 - column 4, line 7	1, 2, 4, 5, 8, 12
Y		7
A		3, 6, 9, 11, 13, 14, 16-20
Y	NOBUYOSHI AWAYA ET AL: "EVALUATION OF A COPPER METALLIZATION PROCESS AND THE ELECTRICAL CHARACTERISTICS OF COPPER-INTERCONNECTED QUARTER-MICRON CMOS" IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 43, no. 8, August 1996, pages 1206-1211, XP000636254 see page 1206 - page 1207, left-hand column see page 1208; figures 3-5	3, 7-12, 14-16, 19
X	US 5 403 434 A (MOSLEHI MEHRDAD M) 4 April 1995 see column 1, line 13 - line 50 see column 4, line 49 - column 5, line 37 see column 6, line 15 - line 46 see column 7, line 65 - column 8, line 31 see column 8, line 44 - column 9, line 30; figure 1 see column 11, line 22 - line 48 see column 13, line 55 - column 14, line 41	1, 4-6
A		3, 7-9, 11-16, 18

-/--

INTERNATIONAL SEARCH REPORT

Inter. Appl. No.
PCT/US 98/23353

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 681 780 A (SHINAGAWA KEISUKE ET AL) 28 October 1997 see column 1, line 5 - line 49 see column 8, line 35 - column 10, line 10; figures 1A,1B,3 see column 10, line 64 - line 67 see column 12, line 1 - column 13, line 51; figures 16A-17B see column 14, line 13 - column 15, line 13	1,2,4
A	---	3,7-11, 14-16
X	YASUDA T ET AL: "DUAL-FUNCTION REMOTE PLASMA ETCHING/CLEANING SYSTEM APPLIED TO SELECTIVE ETCHING OF SiO ₂ AND REMOVAL OF POLYMERIC RESIDUES" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART A, vol. 11, no. 5, 1 September 1993, pages 2496-2507, XP000411304 see page 2496 - page 2497, left-hand column; figure 1 see page 2498, right-hand column, paragraph C see page 2505, paragraph 3 - page 2506, paragraph IV	1,2,5,6
A	---	8,9,12, 14
X	EP 0 680 070 A (TOKYO ELECTRON LTD) 2 November 1995 see column 1, line 1 - line 27 see column 2, line 13 - line 21 see column 4, line 13 - column 7, line 31; figures 1,2,4A-4C,5	1,2,4
A	---	8-11, 14-16
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 311 (E-1561), 14 June 1994 -& JP 06 069168 A (FUJITSU LTD), 11 March 1994 see abstract	1,2,4
A	-----	3,7-9, 11,13, 14,16, 19,20

TC 17 1/6/03

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 98/23353

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0305946	A	08-03-1989	JP 1200628 A	11-08-1989
			JP 1086521 A	31-03-1989
			DE 3855636 D	05-12-1996
			DE 3855636 T	27-03-1997
			US 5298112 A	29-03-1994
			JP 2049425 A	19-02-1990
			JP 2724165 B	09-03-1998

US 5306671	A	26-04-1994	JP 2814021 B	22-10-1998
			JP 4229621 A	19-08-1992
			DE 4122587 A	23-01-1992
			KR 9405281 B	15-06-1994

EP 0518774	A	16-12-1992	FR 2677668 A	18-12-1992
			DE 69208743 D	11-04-1996
			DE 69208743 T	25-07-1996
			JP 5234973 A	10-09-1993

US 5403434	A	04-04-1995	NONE	

US 5681780	A	28-10-1997	JP 8045912 A	16-02-1996

EP 0680070	A	02-11-1995	JP 4206719 A	28-07-1992
			DE 69124672 D	27-03-1997
			DE 69124672 T	19-06-1997
			EP 0488393 A	03-06-1992
			US 5385624 A	31-01-1995

DOCKET NO: GR 20 P 1582
 SERIAL NO: 09/817, 967
 APPLICANT: Lowery et al

LERNER AND GREENBERG P.A.
 P.O. BOX 2480
 HOLLYWOOD, FLORIDA 33022
 TEL. (954) 925-1100